Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **N. 1Q0**
2. **1D0**
3. **1D1**
4. **N. 2E**
5. **VCC**
6. **2D0**
7. **2D1**
8. **N. 2Q1**
9. **2Q1**
10. **2Q0**
11. **N. 2Q0**
12. **GND**
13. **N. 1E**
14. **N. 1Q1**
15. **1Q1**
16. **1Q0**

**49 mils**

**56 mils**

**2 1 16 15 14**

**13**

**12**

**7 8 9 10 11**

**3**

**4**

**5**

**6**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VCC or Isolated**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .049” X .056” DATE: 3/31/16**

**MFG: TIH THICKNESS .011” P/N: 54HC75**

**DG 10.1.2**

#### Rev B, 7/19/02